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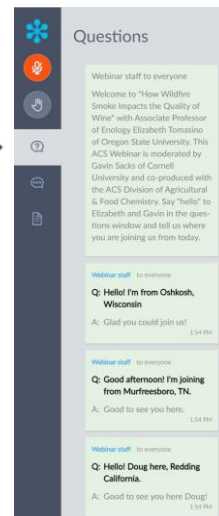


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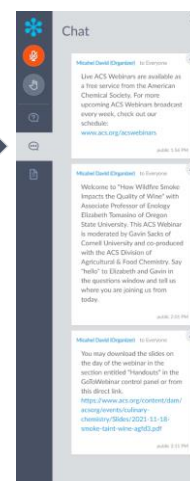
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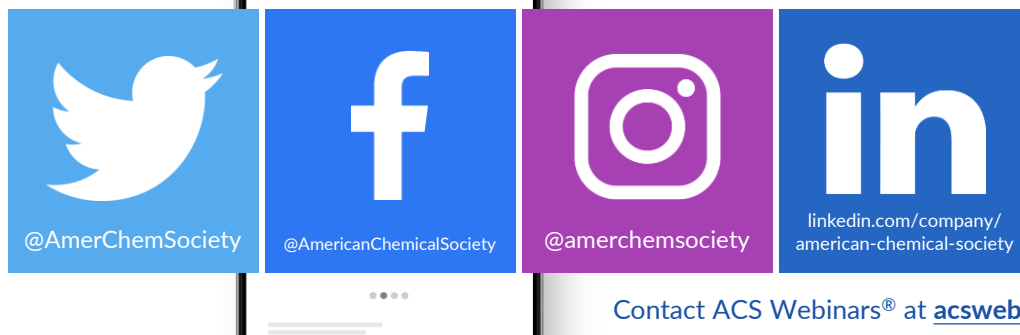


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A Career Planning Tool For Chemical Scientists



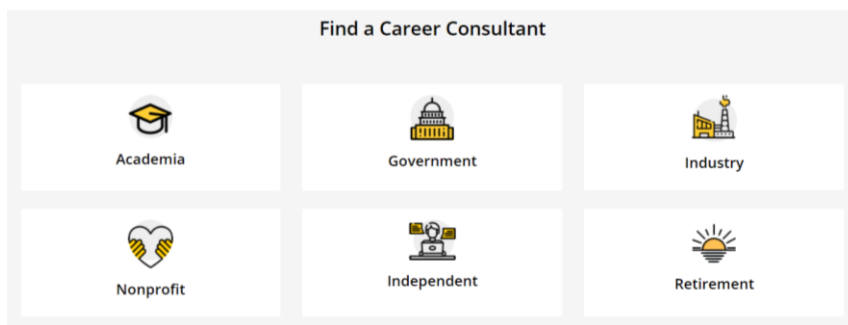
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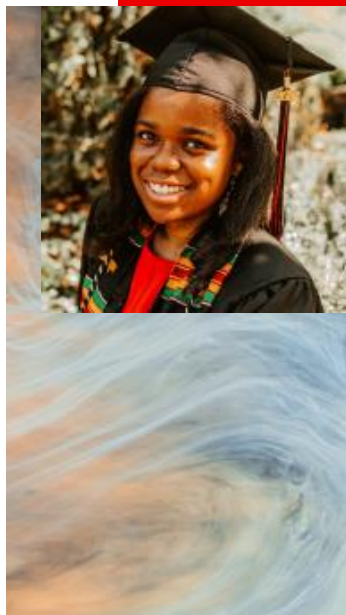
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ACS Scholar Adunoluwa Obisesan

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Advancing ACS' Core Value of Diversity, Equity, Inclusion and Respect



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**Adapted from definitions from the Ford Foundation Center for Social Justice:

Equity**

Seeks to ensure fair treatment, equality of opportunity, and fairness in access to information and resources for all. We believe this is only possible in an environment built on respect and dignity. Equity requires the identification and elimination of barriers that have prevented the full participation of some groups.

Diversity**

The representation of varied identities and differences (race, ethnicity, gender, disability, sexual orientation, gender identity, national origin, tribe, caste, socioeconomic status, thinking and communication styles, etc.) collectively and as individuals. ACS seeks to proactively engage, understand, and draw on a variety of perspectives.

Inclusion**

Builds a culture of belonging by actively inviting the contribution and participation of all people. Every person's voice adds value, and ACS strives to create balance in the face of power differences. In addition, no one person can or should be called upon to represent an entire community.

Respect

Ensures that each person is treated with professionalism, integrity, and ethics underpinning all interpersonal interactions.

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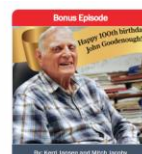
Bonus Episode
Carolyn Bertozzi and K. Barry Sharpless chat about sharing the 2022 Nobel Prize in Chemistry
December 6, 2022



Bonus Episode
Bioorthogonal, click chemistry clinch the Nobel Prize
October 5, 2022



Episode #46
Lithium mining's water use sparks bitter conflicts and novel chemistry
September 13, 2022



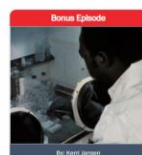
Bonus Episode
Happy 100th birthday, John Goodenough!
For John Goodenough's 100th birthday, Stereo Chemistry revisits a fan-favorite interview with the renowned scientist
July 25, 2022



Bonus Episode
Jesse Wade on Wikipedia and work-life balance
June 21, 2022



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ACS Career Resources



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<https://www.acs.org/careerconsulting.html>

Personal Career Consultations

Jim Tung

Assistant
Lacamas Laboratories

S.S., Biochemistry, University of Oregon
Ph.D., Organic Chemistry, University of Notre Dame

Jim Tung works at Lacamas Laboratories in Portland, OR, currently as a business development manager. He has been with Lacamas for 10 years, working on developing new chemical manufacturing projects. Before that, he was a senior research chemist at Orlite Research in Champaign, IL, performing kilo-scale organic chemistry.

An Oregon native, Jim got his B.S. in biochemistry from the University of Oregon, his Ph.D. in organic chemistry from the University of Notre Dame, with postdoctoral experience at Pfizer's laboratories in La Jolla, CA. He is past chair of the Portland Section of the American Chemical Society and was 2019 general co-chair of NORM 2019. He has interests in process chemistry, labor economics, social media outreach and encouraging career exploration and development for younger chemists.

Ask me about:

- Working in industry
- Applying for academic jobs
- Getting your first job

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Chemistry and the Economy: 2023 Mid-Year Review

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The CHIPS and Science Act: What's in it for the Chemistry Enterprise?



NITIN J. SHAH, BA, MA, PhD
Principal Innovator, MITRE Engenuity



HEATH WEEMS, BS
Advocacy Manager, American
Chemical Society

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The CHIPS and Science Act: What's in it for the Chemistry Enterprise?

American Chemical Society Webinar

Nitin J. Shah
MITRE Engenuity
June 15, 2023



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The CHIPS and Science Act of 2022: The Basics

The CHIPS and Science Act of 2022 directs \$ 280Bn in spending over the next ten years, with the bulk for scientific R&D

~ \$ 200Bn proposed funding in STEM, R&D, and workforce and economic development program authorizations at
The National Science Foundation, US Department of Energy and US Department of Commerce

~ \$ 52Bn has already been appropriated in the CHIPS Act with focus on the Semiconductor industry

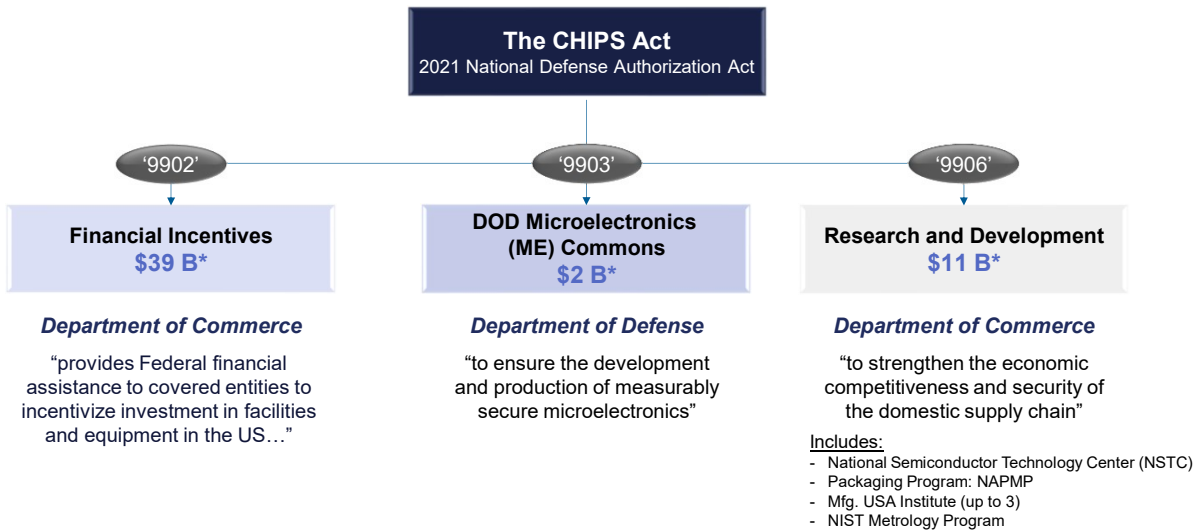
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The CHIPS Act: Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Defense Fund



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*Funding appropriated in the 2022 CHIPS and Science Act



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CHIPS Act R&D Entities: the NSTC and the NAPMP

National Semiconductor Technology Center

- **Oversight:** Led by Sec. of Commerce in collaboration with Sec. of Defense. Industrial Advisory Committee assesses progress.
- **What it is:** a public-private partnership
- **Objective:** Conduct research and prototyping of advanced semiconductor technology to strengthen the economic competitiveness and security of the domestic supply chain
- **Functions:**
 - **R&D:** Conduct advanced semiconductor manufacturing, design and packaging research, and prototyping that strengthens the entire ecosystem
 - **Invest:** support startups with the goal of commercializing innovations
 - **Workforce:** incentivize and expand participation in graduate and undergraduate programs and develop programs and apprenticeships.

National Advanced Packaging Manufacturing Program

- **Oversight:** Established by Sec. of Commerce. Led by Director of NIST, in coordination with the NSTC. Industrial Advisory Committee assesses progress.
- **What it is:** a program
- **Objective:** Strengthen the semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem.
- **Coordination:** Must coordinate with the Manufacturing USA Institute in 9906(f), if it is established.

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The Background to the CHIPS Act

The United States has the highest spend in R&D, education and venture investments.

And yet...

- US share of chip manufacturing has slipped from ~30% in 90s and projected to be 9% by 2030.
- US currently has a market share ~3% in semiconductor packaging
- US has deep strengths in Electronic Design Automation software and semiconductor process equipment supply, enabling the manufacturing of semiconductor products globally
- US lacks the workforce to meet the current and emerging demand for the semiconductor industry

The pandemic and supply chain disruptions have illustrated vulnerabilities:

Supply chain resiliency is needed to strengthen economic and national security

“Getting the R&D infrastructure right will determine our success for decades.”
-Commerce Secretary Gina Raimondo, Industrial Advisory Committee meeting Dec. 8, 2022, Washington D.C.

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Bottom Line Up-Front (BLUF): Over the horizon innovation

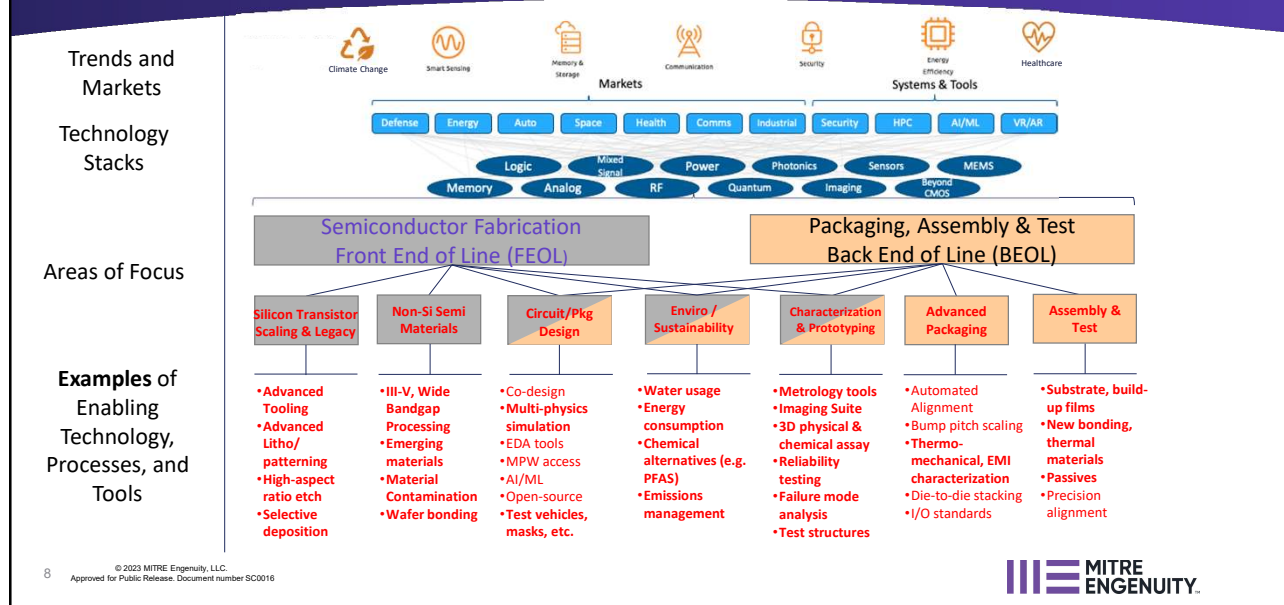
- The CHIPS & Science Act provides a generational opportunity for industry, academia and individuals for imaginative solutions
- For funded programs such as the CHIPS Act, already technology roadmaps are being defined and specific programs established
- This is the time to communicate, collaborate, propose ideas into the marketplace, take lead and address numerous challenges in the develop of chemical processes and solutions for:
 - Processing of Silicon and wide bandgap semiconductors for electronics, optics and other applications: density (2D and 3D patterning), yield, power, sustainability goals
 - Advancement of packaging solutions for microelectronics, photonics and integration, requiring new materials, 2D and 3D patterning, demanding thermal, physical, environmental conditions

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Opportunities for ACS Members to contribute to the CHIPS Act The need for Over-The-Horizon Innovation, Roadmaps, Skills



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Bottom Line Up-Front (BLUF): Over the horizon innovation

- The CHIPS & Science Act provides a generational opportunity for industry, academia and individuals for imaginative solutions
- For yet to be funded programs (the other \$ 200Bn), collaboration between Government, Academia and Industry can drive roadmaps and investment
- Examination of the “& Science” part of the Act illustrates opportunities and challenges and the broad objectives
- This is the time to collaborate and educate government on the possibilities
- And to gear up with training, skills and enthusiasm to build critical mass of talent

9



9

Introduction to MITRE and MITRE Engenuity

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MITRE solves problems for a *safer world*, through federally funded research and development centers and public-private partnerships.

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A Vision for the National Semiconductor Technology Center

A vision for how the US intends to leverage Incentives and R&D funds to strengthen supply chain and national security (white paper published November 2021)


KEY THEME: A Marketplace of Ideas

- **Breakthrough Challenges and Full Stack Innovation:** market and technology goals
- **Nationwide Network** of new and existing facilities, infrastructure, tools, metrology
- **Strategic Investment Fund** capital and incubator for de-risking investments
- **Domestic semiconductor Workforce** at all skill levels and stages of career
- **Effective Governance** addressing openness, conflicts, and intellectual property
- **Coordination with existing and future U.S. government programs**


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The Semiconductor Alliance's Work to Date



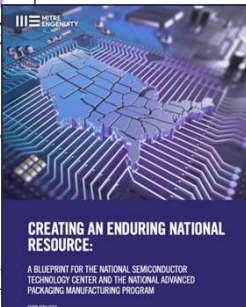
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Jun – Nov 2021



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Jan – Mar 2022



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Objectives for NSTC

- Lower barriers for access
- Create value for the ecosystem
- Build trust through neutrality
- Full-stack, system-level approach
- Whole-of-nation engagement

Key Tenets for an Impactful NSTC

- Effective and neutral governance
- Ambitious technology agenda
- A robust network and operating model
- Long-term financial sustainability
- Targeted workforce development
- Integrated startup investment fund

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Circuit Talk: Full Stack

VIDEO SERIES
CIRCUIT TALK FULL STACK

Simplifying complex semiconductor thought, this informal video series spotlights experts exploring deep technical concepts in short, meaningful bites.


Hosted by **Nitin J. Shah**
Principal Innovator, MITRE Engenuity



 <p>EPISODE 4 ELECTRONIC DESIGN AUTOMATION (EDA), EQUITY, AND EXPANSION IN THE CLOUD</p> <p>Guest(s): Deirdre Hanford <i>Chief Security Officer, Synopsys</i></p>	 <p>EPISODE 3 WORKFORCE DEVELOPMENT AND ADVANCED PACKAGING</p> <p>Guest(s): Jim Vandever <i>President, BRIDG</i></p>	 <p>EPISODE 2 THE FUTURE OF THE SEMIVERSE</p> <p>Guest(s): Rick Gottscho <i>Executive Vice President and Chief Technology Officer, Lam Research</i></p>	 <p>EPISODE 1 AN INTRODUCTION TO FULL STACK INNOVATION</p> <p>Guest(s): Todd Holmdahl <i>Corporate Vice President, Microsoft</i></p>
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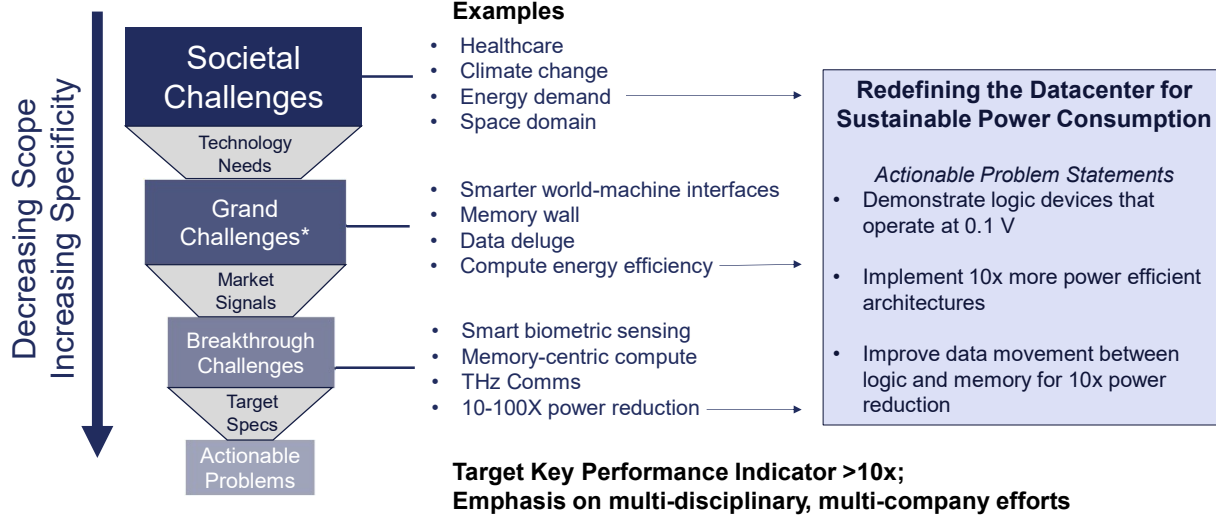
<https://mitre-engenuity.org/semiconductors/circuit-talk/full-stack/>

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Making Market-Driven Breakthrough Challenges Actionable

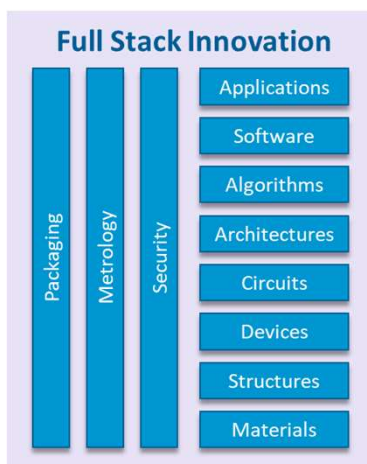


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Innovation: Full Stack Innovation



The future will be shaped by those who understand full stack innovation and implications for the market, supply chains and external factors

- Historically the industry grew by cooperation by partners in vertical integration and supply chain
- Over time, the industry has grown at all layers of the stack e.g. *fabless, Electronic Design Automation, foundries, materials providers, tools and patterning*
- Hennessy and Patterson: prediction that the next generation of products will require companies to innovate at all layers of the stack to achieve major breakthroughs



<https://www.acm.org/hennessy-patterson-turing-lecture>

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SIA/Semiconductor Research Corporation Decadal Plan

Five Seismic Shifts That Will Define The Future of Semiconductors and ICT



1. Fundamental breakthroughs in analog hardware are required to generate smarter world-machine interfaces that can sense, perceive, and reason. Annual investment need: \$600M throughout this decade to pursue analog-to-information compression/reduction with a practical compression/reduction ratio of 10⁵:1 for practical use of information more analogous to the human brain.



2. The growth of memory demands will outstrip global silicon supply, presenting opportunities for radically new memory and storage solutions. Annual investment need: \$750M throughout this decade to develop emerging memories/memory fabrics with >10-100X density and energy efficiency improvement for each level of the memory hierarchy. Discover new storage systems and storage technologies with >100x storage density capability.



3. Always-available communication requires new research directions that address the imbalance of communication capacity vs. data-generation rates. Annual investment need: \$700M throughout this decade for communication enabling data movement of 100-1000 zettabyte/year at the peak rate of 1Tbps@ <0.1nJ/bit. Develop intelligent and agile networks that effectively utilize bandwidth to maximize network capacity.



4. Breakthroughs in hardware research are needed to address emerging security challenges in highly interconnected systems and AI. Annual investment need: \$600M throughout this decade for privacy and security hardware advances that keep pace with new technology threats and use cases (e.g., trustworthy AI systems, secure hardware platforms, and emerging postquantum and distributed cryptographic algorithms).



5. Ever-rising energy demand for computing vs. global energy production is creating new risk, and new computing paradigms offer opportunities to dramatically improve energy efficiency. Annual investment need: \$750M throughout this decade to discover computing paradigms/architectures with a radically new computing trajectory demonstrating >1,000,000x improvement in energy efficiency.

SIA/SRC Decadal Plan for Semiconductors - <https://www.src.org/about/decadal-plan/>

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Five Seismic Shifts shared with permission from David Henshall at SRC



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Mega-Trends: External Factors in the Semiconductor Market

Questions that face our industry and its future:

- **Talent**
 - How can we encourage the next generation to be excited about working in our industry?
 - What are the skills required for the next few decades?
- **Power**
 - How will we generate reliable power to run our fabrication facilities?
 - How can we continue to reduce the power required to operate our products?
- **Sustainability**
 - How can we reduce our impact on the environment (e.g. elimination of PFAS)?
 - What can we do to reduce the long-term effects of our products and materials?

1 - [Public Statement of the Semiconductor PFAS Consortium - Semiconductor Industry Association \(semiconductors.org\)](#)

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Market Growth: Continued Growth of Current Segments

What current product segments will sustain and grow in the next decade?

- **Computing**
 - Data centers, edge, everything
 - Driven by power but also software efficiency and architectures
 - **Memory**
 - Cost, density
 - **Communications**
 - Wireless, optical, wired
- Major trend: advanced packaging:
tension between Moore's Law approach to next node vs heterogeneous integration and customization

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Market Disruptions: Transformation of the Market

How will the industry go from \$ 500Bn to > \$ 1Tn in the next decade?

What will we sell and to whom?

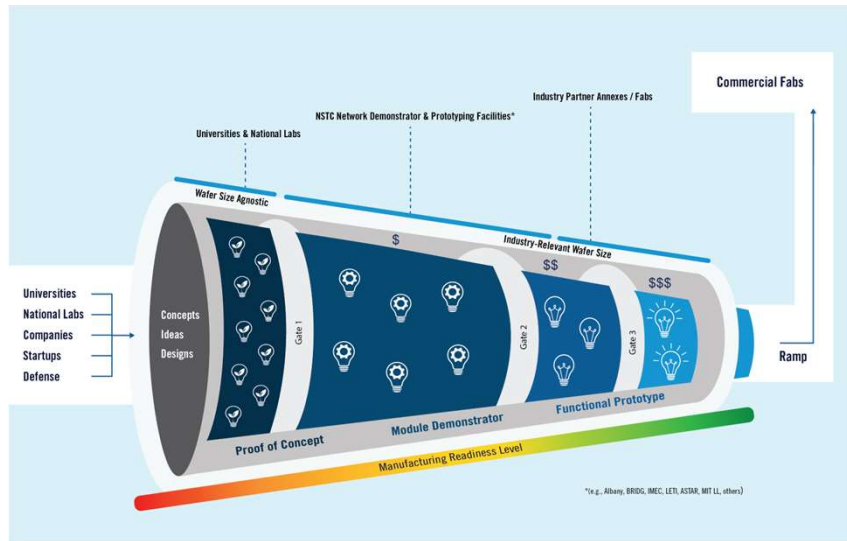
- **Things**
 - Transportation: automotive, aeronautics, personal vehicles
- **Spaces**
 - Home, public places, cities, professional and medical spaces
- **Industry**
 - Automation, robotics, manufacturing
- **Medical**
 - Personal care, professional, physical and mental
- **Education/Media/Platforms**
 - Virtual, augmented and mixed reality, enhanced communications and sensing

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Innovation: Lab to Fab

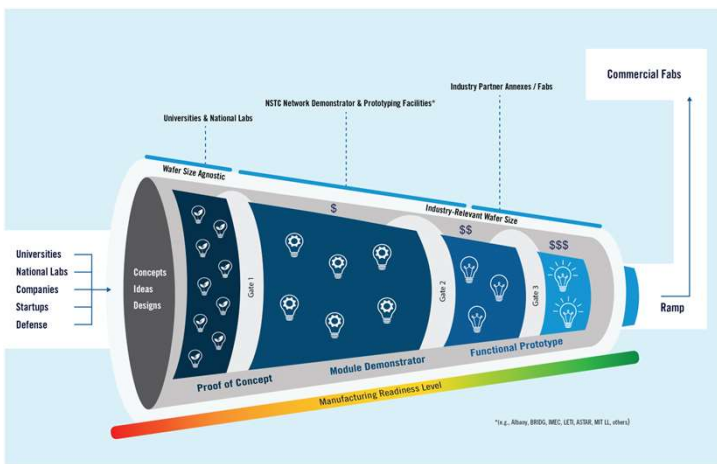


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The NSTC's Role in Lab-to-Fab Transition



Stages of Development

Proof Of Concept

- Basic R&D
- Scientific Understanding
- Novel concepts/methods/designs
- Common baselines & test structures

Module Demonstrator

- Concept hardening
- Industry relevant baselines
- Module/test site demonstration

Functional Prototype

- Prototypes
- Functional check

Ramp

- Transition tech to commercial partners

NSTC's Focus

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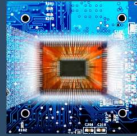


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An Emerging Opportunity: Advanced Packaging

National Advanced Packaging Manufacturing Program

- **Oversight:** Established by Sec. of Commerce. Led by Director of NIST, in coordination with the NSTC. Industrial Advisory Committee assesses progress.
- **What it is:** a program
- **Objective:** Strengthen the semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem.
- **Coordination:** Must coordinate with the Manufacturing USA Institute in 9906(f), if it is established.



NIST Webinar October 18th, 2022
 “CHIPS for America Strategy Paper Briefing – R&D Programs”

NATIONAL ADVANCED PACKAGING MANUFACTURING PROGRAM



- To expand and grow U.S. capacity in advanced packaging
- Capture available market share in packaging revenue
- Pilot facility for testing and integration of new processes
- A network of public private partnerships with universities, industry, and other government agencies focused on a range of issues including:
 - Substrate technology
 - Heterogeneous integration
 - Wafer and panel-based approaches
 - Tooling and automation

National Institute of Standards and Technology | U.S. Department of Commerce 18



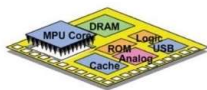
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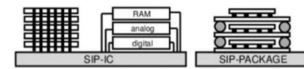
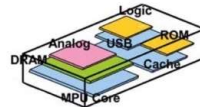
Industry Roadmap: “More Moore” to “More-than-Moore”

Transistor Scaling: System on Chip

Apple M1 Ultra – 114 bn transistors
 864 mm² (19.3 x 44.8)



Advanced Packaging: Heterogeneous Integration



- Multiple components onto a single **chip**
- Low flexibility
- Longer time to market
- All components manufactured at **same** node
- Large chip size, low yield, increased cost

- Multiple components into single **package**
- High flexibility
- Shorter time to market
- Components manufactured at **any** node
- Smaller chip-’let’ size, higher yield, decreased cost

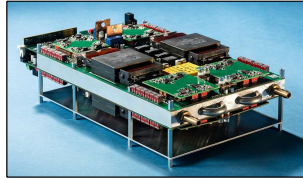
The *transistor scaling* approach of the past few decades will be transitioning to a *systems approach* through **Advanced Packaging & Heterogenous Integration**

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Future Technologies Enabled by Advanced Packaging



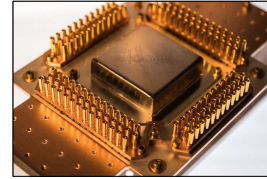
WBG & Power

- Thermal management
- HV materials
- Improved reliability



Neuromorphic Computing

- Reconfigurability
- Weighted connections



Quantum Computing

- Cryogenic operation
- Low-loss RF and Optical coupling
- Chip-to-chip entanglement

Advanced packaging will require innovations in materials, patterning, 3D structures, new process and manufacturing techniques, measurement and characterization, automation, data analytics and tools

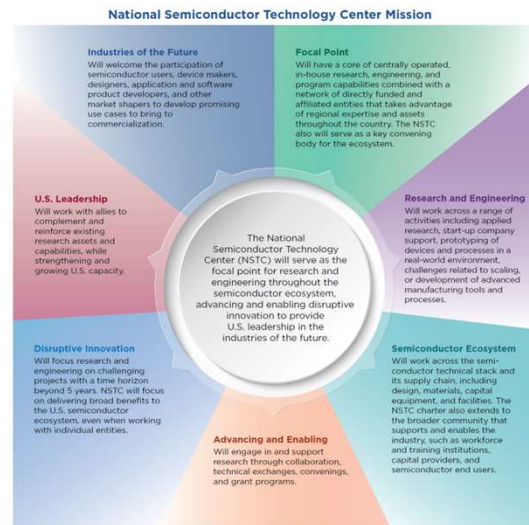


National Semiconductor Technology Center: “Focal point for research and engineering throughout the semiconductor ecosystem”

<https://www.nist.gov/chips>



The US CHIPS Act: R&D Highlights
 Manufacturing USA
 Metrology Research
National Semiconductor Technology Center (NSTC)
 National Advanced Packaging Manufacturing Program (NAPMP)



National Institute of Standards and Technology: <https://www.nist.gov/>



NIST Whitepaper on the NSTC: Overview

- Department of Commerce anticipates the creation of a new, purpose-built, independent, nonprofit entity with the requisite neutrality, expertise, leadership, and capacity to serve as the operator of the NSTC.
- Three Programs: Technology leadership; Managing assets that benefit the community; Workforce programs
- A “whole-of-government approach”

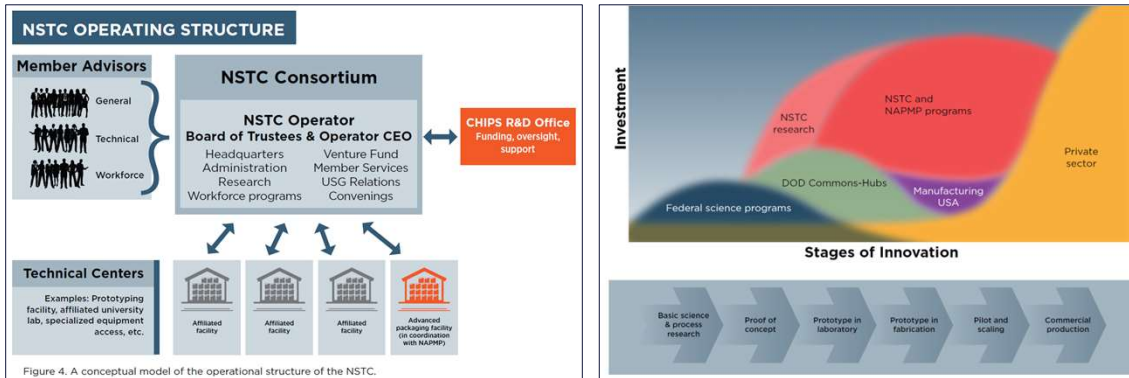


Figure 4. A conceptual model of the operational structure of the NSTC.

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NIST Whitepaper on the NSTC: Community Input

Technical Centers (page 15)

Design Enablement Gateway (page 16)

Membership Structure (page 20)

TECHNICAL CENTERS: COMMUNITY INPUT
 The semiconductor community has provided extensive input to the requirements for potential technical centers. The NSTC will engage in a prioritization process to ensure that the highest priority needs are met with the funds available. Identified needs for the NSTC to consider include:

- Scalable CHIPS (complementary metal-oxide semiconductor) Fully functional and supported CHIPS process flow at 22 nm or below with a capacity of 10,000 wafers starts per month on 300 mm wafers
- CHIPS R&D process: Front-end short loops supporting < 3 nm technology R&D at a capacity of 2,000 wafers per month using extreme ultraviolet technology enabling the development of leading-edge materials, devices, and process and metrology tools
- Manufacturing test vehicles that provide low-cost patterned and functional substrates that can be used to provide data through electrical test, to enable materials, equipment, process, and device development and optimization, especially for CHIPS-enabled technologies
- Extended metrology capacity to enable R&D in a production environment including rapid fabrication to enable prototype development cycles, enhance in-line process monitoring capabilities, and on-line characterization facilities
- Space and flexibility to accommodate next-generation or prototype processing and metrology tools as they can be demonstrated in a production environment
- Back-end short loop processing from specialized capabilities enabling “fab-to-fab” finishing of R&D devices and high-quality processing of novel materials and devices while maintaining process and material integration
- Power electronics: Power management devices often require non-SiC02 substrates (e.g., silicon carbide, gallium nitride) and specialized designs, tools, and processes
- Back frequency mixed signal and analog characterization and testing capabilities require diverse capabilities distinct from leading-edge CHIPS
- Photonics: Advancements in quantum sensing and interconnect are all possible at the intersection of light and electronics
- Microelectromechanical systems: Sensors for mobile, automotive, health care, and internet-of-things are all growth areas that require resources distinct from traditional CHIPS flow
- Biotechnology: The convergence of microfabrication and biotechnology brings new opportunities, but also increased complexity and significant integration challenges
- Future nodes: The NSTC may seek to have capacity at a node node (e.g., 10 nm), with such a facility well suited to certain research programs and workforce education
- Design tools: New design tools and methodologies to accelerate the generation of circuit IP, virtualize devices, circuits, and processes, and enable co-design, simulation, and heterogeneous integration

DESIGN ENABLEMENT GATEWAY: COMMUNITY INPUT
 The semiconductor community has provided extensive input to the requirements for a new hosted design ecosystem. Specifications that have been identified include:

- A complete set of resources needed for the design, simulation, and tape-out of integrated systems to be made in the US, without proprietary information leaving the cloud environment
- A well-structured, secure-controlled discharge system between all participants within a multi-party, multi-tenant, multi-tenant ecosystem to facilitate design IP as needed by the members
- An “open” like environment where users can exchange integrated circuit design IP under standardized licensing and support terms for basic R&D as well as for commercial use, as determined by the owner of the circuit design IP
- A catalog of IP generated from NSTC-sponsored projects, along with a pre-defined set of contractual obligations to determine the ownership of that IP (it may be owned or co-owned by members or the NSTC itself)
- A catalog of circuit design IP from NSTC-sponsored projects and, to the extent possible, of other federal agencies, that is made available for license at a reasonable cost
- A resource to help ease the provenance of circuit design IP both to ensure it is secure and to prevent any of proprietary information
- Collaboration between commercial EDA, vendors and universities or startups to consider integration, via industry standard tool formats or discipline engineering interfaces (APIs) that would allow EDA innovations (open source or proprietary) to more tightly integrate and leverage commercial tool investment, education, and support

The community has suggested options in licensing that the NSTC could consider in partnership with providers of EDA training and integrated IP:

- Enabling the contribution of circuit design IP under standard contributor license agreements
- Allowing NSTC members to access NSTC EDA resources using their own existing licenses (“bring your own license”)
- Subsidizing EDA and circuit design IP license access for U.S. government agencies, universities, and early-stage startups
- Developing, promoting, and supporting existing or new licensing models that improve community access, such as a non-commercial, research-only license at low or no cost

MEMBERSHIP STRUCTURE: COMMUNITY INPUT
 The following benefits have been requested as part of the membership structure, and could be included either in the base fee or as an add-on cost:

- Use of technical centers
- Access to research and development programs, technical expertise, emerging materials and process technologies, and manufacturing test vehicles
- Access to digital assets, such as EDA and design enablement tools, IP, and aggregated data sets
- Facilitated access to multi-project wafers at leading-edge and mature foundries
- Access for startups to a nurturing ecosystem, including resources such as incubation support, IP-licensing guidance, conveying opportunities that introduce startups to interested investors, and coordination with the efforts of other federal agencies
- Participation in the groups that advise the NSTC leadership on different program objectives
- Participation in industry coverage including groups focused on tool issues, standards, and grand challenges
- Participation in training, workforce development, technical exchange programs, and access to the workforce data clearinghouse

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Profile of the Global CHIPS Acts

Country	Objective	Incentive Amount (\$B)	Date passed
US	Bolster U.S. leadership in semiconductors	\$52B	Aug 2022
China	Counter U.S. moves aimed at slowing its technological advances	\$143B	Dec 2022
South Korea	"K-Semiconductor Belt" strategy: Become a comprehensive (beyond memory) semiconductor powerhouse by 2030	25% R&D tax credits 5% Capex tax credit	May 2021
Taiwan	Encourage semi manufacturers to invest in facilities & new technologies	- Up to 40~50% tax credit for R&D - Up to 10~20% tax credit for facility investments	Jan 2023
India	Position India as global hub for electronics manufacturing	\$10B	Dec 2022
Japan	Double domestic chip revenue to \$114 billion by 2030	\$6.8B	2021/2022
European Union	Double the EU's current 10% share of the global semiconductor market by 2030	\$30B - \$50B	Feb 2022

- Multiple nations are providing incentives for the Semiconductor industry
- Factors affecting government actions
 - Driven by Pandemic and Disruption to Global Supply Chain and resulting Economic Impact

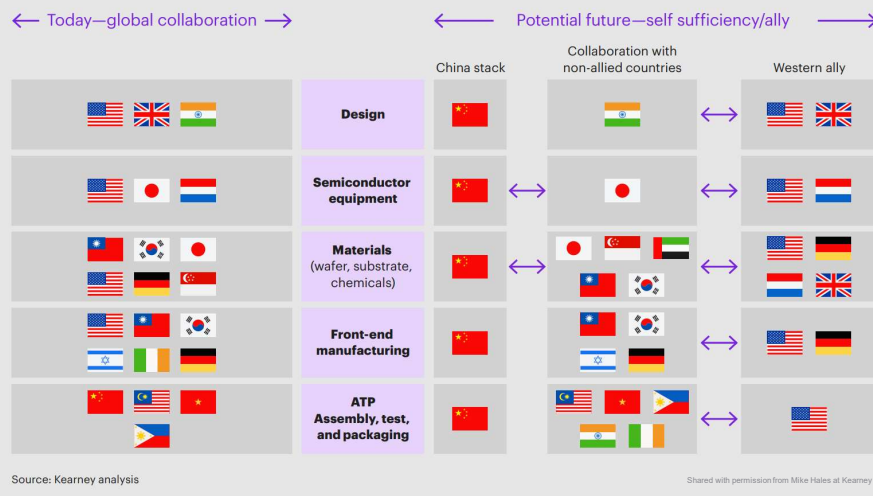
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Global Supply Chain and Alliances

Global industry collaboration in semiconductors—current and potential future scenario



Source: Kearney analysis

Shared with permission from Mike Hales at Kearney

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<https://www. Kearney.com/industry/technology/article/-/insights/why-a-resilient-semiconductor-supply-chain-is-imperative-and-how-to-create-one>



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CHIPS Act Summary

Topics to consider to meet the global market demand for semiconductor products

- What is the best path for industry to align with government actions?
- How to respond to the changes in the market?
- How to attract the best technical and business talent to our industry?

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Opportunities for ACS Members to contribute to the CHIPS Act

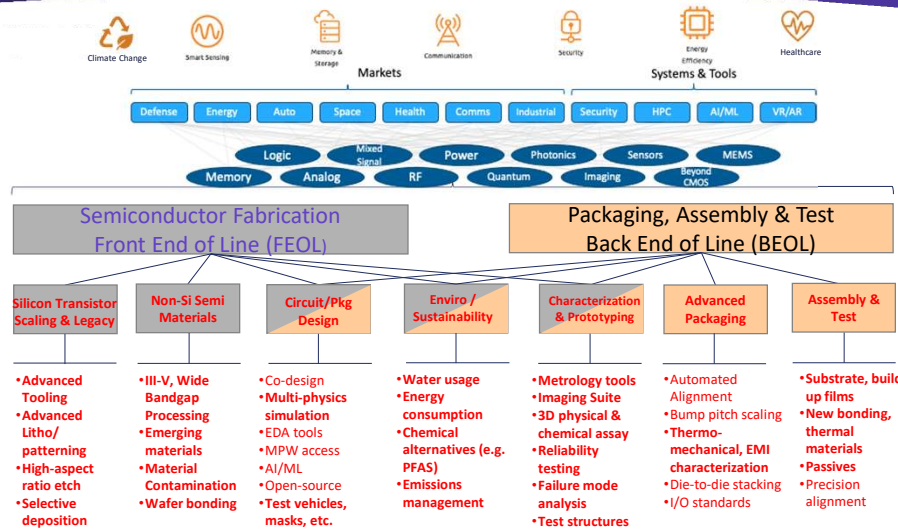
The need for Over-The-Horizon Innovation, Roadmaps, Skills

Trends and Markets

Technology Stacks

Areas of Focus

Examples of Enabling Technology, Processes, and Tools



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Nitin J. Shah

nshah@mitre-engenuity.org

- Nitin J. Shah is an innovator, with over 35 years of experience in technology development, corporate and product strategy, marketing, and business development.
- Currently Nitin is Principal Innovator at MITRE Engenuity, a not-for-profit tech foundation for the public good, and is based in Silicon Valley.
- He is a leading architect of the MITRE Engenuity proposal for the National Semiconductor Technology Center and worked with corporations, start-ups, academia and financial institutions, to craft a position in support of the CHIPS Act and the resurgence of the US semiconductor industry.
- Previously, he orchestrated the successful proposal to NASA for an award to Nokia for deployment of first ever 4G/LTE network on the lunar surface. Nitin was in Nokia's Tech Ventures initiative, to commercialize IP and technology from Bell Labs via partners and incubators.
- Nitin's career spans AT&T Bell Labs, Lucent Technologies, Nokia Bell Labs, several start-ups, and providing consulting and decision services for clients such as DoCoMo, Ericsson, and Intel. He has expertise in mobile networking, digital media, consumer privacy and semiconductors.

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Final Thoughts and Takeaways

- ***What is in the CHIPS and Science Act and what will it mean for the chemical enterprise:***
 - A Generational opportunity to accelerate innovation and manufacturing
- ***Insights into future directions of U.S. funding agencies like NSF, NIST, and DOE:***
 - Emphasis on workforce, a rich marketplace of ideas
 - Alignment and commitment by academia and industry to leverage the new funding
- ***How this legislation seeks to address science and technology challenges of the future, and how other countries are responding:***
 - We are in a global ecosystem where choices are going to be dictated by complex issues related to the supply chain, allies and collaborations, and broader issues of sustainability, climate and the environment

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in the questions window!

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Final Thoughts and Takeaways

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